Low Temperature Characterization of Ta/InAs and Al/Si/Al Josephson Junctions With Single Crystalline Barriers

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Quantum computers have the power to transform computing with their potentially faster computation times due to their use of quantum bits, qubits. Superconducting qubits are particularly promising as they make use of a superconducting quantum LC circuit, swapping the linear inductor with a nonlinear inductor, a Josephson junction. Josephson junctions introduce anharmonicty to our system, allowing for a two state system with selectable and tunable quantum states. Transmon qubits, essentially junctions in parallel with a capacitor, operate in this slightly anharmonic regime. In this paper we utilize low temperature characterization techniques to characterize various Josephson junctions each tackling current qubit design and material challenges in the field. Merged-element transmon qubits (METs) utilizing a single crystalline barrier are a promising avenue to potentially reduce losses while also merging the external capacitor and Josephson junction into a single element. Such can be realized with Al/Si/Al junctions where the Si layer is on the order of $\sim$ 10 nm. Specifically, we probe tunneling properties of these junctions. On the other hand, gate tunable transmon qubits known as gatemons allow for frequency tunable qubits which is desirable for certain computational tasks. Josephson junctions with a semiconducting barrier material are a unique superconductor-semiconductor system with applications to these gatemons, where an applied gate voltage alters the conductivity in the semiconductor region, and allows for control over the frequency of the qubit. Here, we study such a junction composed of Ta/InAs and investigate tunability. Additionally, we analyze the quality of our Ta/InAs junction, using the product of the critical current (I_c) and the normal state resistance (R_N), of 4.4 mV, along with the observation of multiple Andreev reflections to confirm high sample quality which is imperative for practical devices.

I. INTRODUCTION

The first successful implementation of a quantum algorithm by Shor *et al.* [1] highlight a promising future of quantum computers outperforming their classical counterparts in certain areas. Particularly interesting areas include combinatorics [2], cryptography [1], and quantum simulation [3]. Quantum simulation is of particular interest to quantum chemists, possibly providing solutions to unanswered questions in quantum chemistry [4], perhaps aiding in drug discovery.

Quantum computers operate according to the rules of quantum physics, a drastic change from classical computers obeying classical physics. Rather then operating on the classical bit of either 0 or 1, these computers make use of the quantum bit (qubit) represented by some two state system with eigenstates $|0\rangle$ and $|1\rangle$, allowing for a superposition of both states. Exploitation of quantum principles for quantum computing applications presents a formidable scientific and technological challenge. How can we construct a qubit system isolated from the environment, but inter-coupled allowing for computation?

An approach to this is the use of quantum integrated circuits, where qubits are constructed from circuit like electrical elements, promising for their large electromagnetic cross sections, allowing for easier qubit coupling [5]. To behave quantum mechanically, absence of dissipation is a requirement, and can be achieved by cooling to superconducting temperatures. Ordinary superconducting quantum LC circuits shown in figure 1(a) creates energy eigenstates seen in figure 1(b) where the energy levels are equally spaced. This poses problems for potential qubit applications as there is no tunability between specific quantum states, creating difficulties in quantum state preparation.

Quantum circuits shown in figure 1(c) are promising superconducting qubit candidates as they provide essential nonlinearity in the form of a nonlinear inductor, a Josephson junction (JJ). Josephson junctions are essential components of superconducting qubits as they introduce anharmonicity as shown in figure 1(d) where the energy levels are unequally spaced, allowing for the creation of a distinct computational subspace and selectability over specific states. Here, we characterize various types of

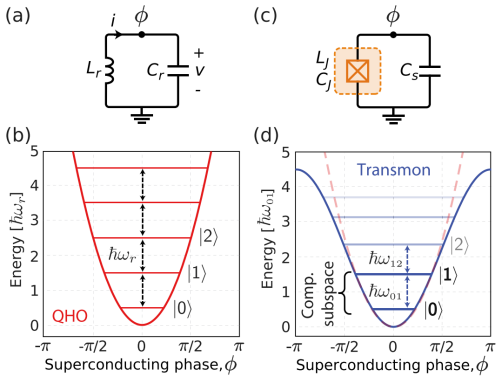

FIG. 1. Superconducting circuits and their corresponding energy diagrams. (a) Superconducting quantum LC circuit with superconducting phase, ϕ, inductance L_r, and capacitance C_r. (b) Energy potential for figure 1(a). Closely resembles that of a QHO with equal energy spacing. (c) Superconducting quantum circuit with a nonlinear inductor (a JJ) with a superconducting phase, ϕ, inductance L_j, and capacitances C_j and C_s. (d) Energy potential for figure 1(c) where the JJ has introduced anharmonicity to the potential resulting in energy levels with unequal spacing. Figure taken from Ref. [6].

JJs leveraging a single crystalline barrier, promising for potentially decreasing qubit loss, rather than the commonly used amorphous barrier. A mechanism for loss with amorphous materials stems from two-level systems where certain energy states absorb energy close to qubit LC resonance, often times in the microwave regime. The single crystal dielectric is expected to have fewer defects that can absorb microwave radiation, will therefore have fewer states for microwave absorption and hence less loss. On another note, both junctions also exhibit unique, emergent properties tackling current challenges in qubit design and material with applications to different classes of superconducting qubits.

Transmon qubits, a class of superconducting qubits operating in the anharmonic regime, are promising, but difficult to scale towards multi-qubit processors for a multitude of reasons. For example, the interfaces, surfaces, and bulk of both the junction and capacitor of these qubits can contribute to loss, and while these losses can be diluted with larger external capacitors, they greatly increase the qubits physical footprint [7, 8]. Efforts by Ref. [9] have shown a viable alternative qubit, dubbed MET (merged element transmon), where the external capacitor and JJ are merged into a single device.

Merged element transmon (MET) qubits employing a single crystalline barrier are particularly intriguing for their low loss nature while also merging the external capacitor and JJ into a single device. Additionally, this device drastically reduces the qubits footprint. A MET device could be realized with a single crystalline Si fin fabricated from floatzone Si on the order of ~ 10 nm acting as the barrier, with superconducting Al on both sides of the fin.

Gowswami *et al.* [10] developed a process to create a thin vertical Si fin, allowing for angled deposition of Al on both sides, and showed capacitive properties for a fin thickness of approximately 50 nm; however further thinning of the Si fin, not done by Goswami *et al.*, before Al deposition is essential to enter the tunneling regime. Due to its shape and function, it was dubbed the FinMET. In this paper, we probe tunneling characteristics of Al/Si/Al junctions with promising application towards FinMET devices.

While Al/Si/Al junctions are promising, they are fixed frequency qubits, and it is often desirable to tune the qubits frequency. Such an example could be fast gate implementation with high fidelity [6]. An approach to the fixed frequency problem is to replace the barrier material of a Josephson junction within a superconducting quantum LC circuit with a semiconductor, creating a Josephson junction field effect transistor (JJ-FET). The coupling of a superconductor and semiconductor allows for a unique system where superconducting properties can be harnessed in tandem with the tunability offered by a semiconductor [11]. This provides the means to control the conductivity in the semiconductor region via an applied gate voltage [12], allowing for the manipulation of the critical current, I_c.

The critical current is the maximum amount of supercurrent that can flow through the junction and is a parameter playing a role in the determination of the qubits frequency. A Ta/InAs Josephson junction could play the role of a JJ-FET, with potential applications to these gate tunable transmon qubits, known as gatemons. Previous work has been done on Al/InAs junctions [12, 13], but Ta is a promising superconducting material gaining traction in other superconducting applications for its critical temperature of approximately 4.4 K. Moreover, the native oxide of Ta is known to be less lossy then other superconducting materials like Al, Nb, and TiN [14, 15].

Specifically, we utilize low temperature transport characterization in an effort to examine tunability in our Ta/InAs junctions while also characterizing sample quality using the product of the critical current and normal state resistance, I_cR_{N}, along with the observation of multiple Andreev reflections. Andreev reflection involves the conversion of an electron into a hole with opposite spin upon reflecting from a superconductor interface [16], with multiple instances of this process classified as multiple Andreev reflections (MAR). Such a process aids in the characterization of superconductor-semiconductor (S-Sm) interfaces, crucial for determining superconductor properties bestowed upon the semiconductor [17–19]. Ultimately, we conclude high sample quality, crucial for practical superconducting heterostructures discussed here.

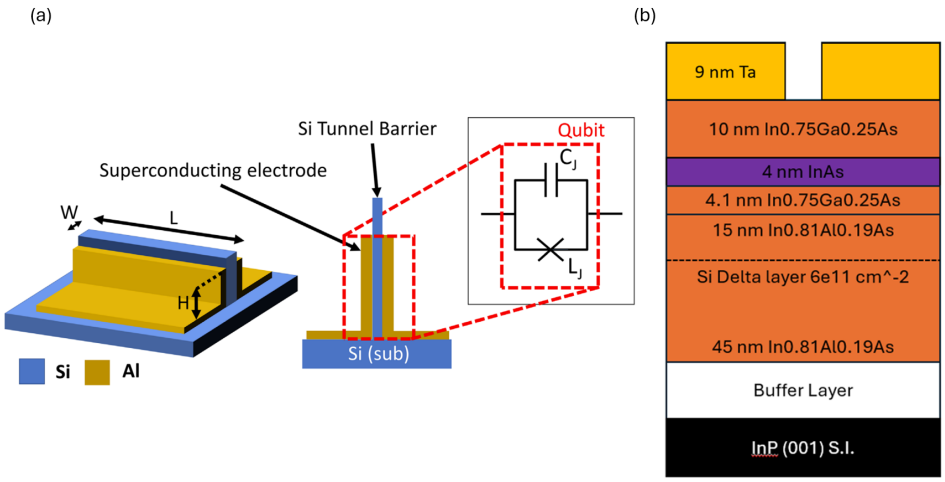

FIG. 2. Illustration of junctions studied in this paper. (a) Schematic of the silicon FinMET with superconducting Al on both sides, where the external capacitor and junction have been merged into a single element. Figure taken from Ref. [10]. (b) Schematic of Ta/InAs JJ grown on InP (001) substrate.

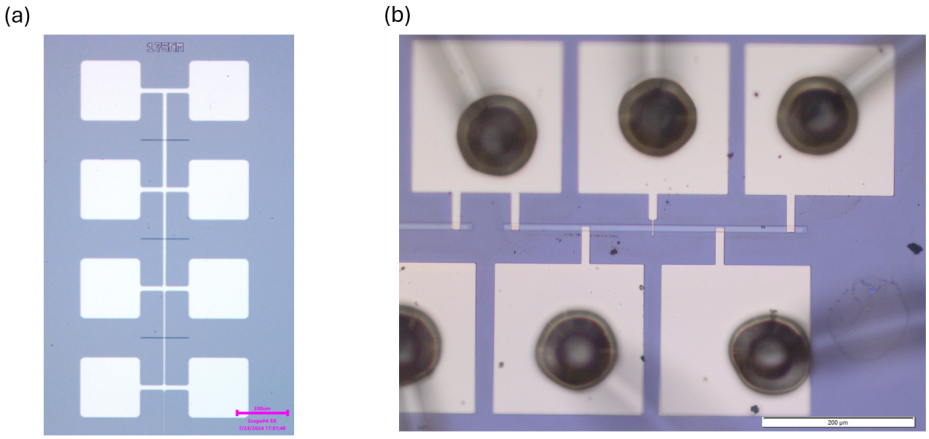

FIG. 3. Optical microscopy images of the samples measured in this paper. (a) Al/Si/Al Josephson junctions with four Ti/Au contacts (white squares) The dark blue horizontal lines are Si fins of approximately uniform thickness across all samples. Vertical white lines represent Al leads, with various thickness indicating various junction area (b) Ta/InAs Josephson junction with five Ti/Au gold contacts. The horizontal strip is our Ta lead, with a fifth contact bring placed over the semiconductor.

II. METHODS

A. Al/Si/Al Josephson Junction

Figure 2(a) shows a 3D schematic of our Al/Si/Al JJ. The fabrication process first begins with a commercially available, low loss Si (110) substrate, with a low stress SiN_x layer being deposited on top with a low pressure chemical vapor deposition (LPCVD) technique. A mask is lithographically defined using electron beam lithography (EBL), followed by a dry etch of the SiN_x. Subsequent anisotropic wet etches of the Si preferentially etch the $\langle 110 \rangle$ direction over the $\langle 111 \rangle$ direction, and creates a Si fin with a SiN_x overhang at the top of the fin. The full fin fabrication recipe can be found in Goswami *et al.* [10] and creates fin thickness of 50-100 nm.

In order to reduce the fin thickness to 10 nm, nescesarry for capacitive and tunneling properties, we use additional techniques. Specifically, we enable oxidation on the Si (111) surface on the order of a few nanometers, and subsequently wet etch the oxidized layer. Such a process allows for the desirable 10 nm thickness, but requires many cycles of etching to achieve. There are other possible techniques, such as a rapid thermal annealer, allowing for a thicker oxidized layer, drastically reducing the total number of etching cycles. Once the Si fin is of

the desired thickness, we use an angled molecular beam epitaxy (MBE) deposition technique to deposit Al onto the sides of the silicon fin. Due to the undercut of the SiN_x, a shadow is formed that prevents the junction from shorting over the top.

B. Ta/InAs Josephson Junction

Figure 2(b) shows the schematic of our Ta/InAs JJ. All samples were grown on semi-insulating InP (001) substrate via MBE. The Ta top layer was grown with a shadow mask technique to avoid etching, and serves as the two superconducting islands of our JJ. Islands are separated by ~ 300 nm gap. The subsequent trilayer constitutes a quantum well, where a smaller bandgap material, InAs, is sandwiched between a material of a larger bandgap, InGaAs. In one dimension, charge carriers are trapped via this quantum well, while the other two dimensions can be treated as a free electron gas (2DEG). Strong coupling between the 2DEG and the Ta is a requirement for the fabrication of a JJ-FET, as JJ-FETs make use of the proximity effect where superconducting Cooper pairs tunnel through the semiconductor region [12].

Electron mobility is also an important consideration when fabricating JJ-FETs. While a thinner top layer of InGaAs may induce stronger coupling it introduces a scattering mechanism, diminishing electron mobility. It has been well noted when taking these two elements into consideration, a 10 nm top layer of InGaAs seems to lead to sufficient mobility and coupling [12, 13, 20]. The layers beneath the quantum well help to confine our potential, minimize growth defects by gradually shifting the lattice constant, and the silicon layer donates charge carriers to the well. For detailed growth on tantalum thin films used in this paper, consult Ref. [14].

C. Low Temperature Measurements

Measurements of all samples were taken below superconducting temperatures in an adiabatic demagnetization refrigerator (ADR) enabling temperatures as low as 50 mK with DC electrical properties measured with a 4-point resistance to ensure only sample resistance was measured. Figure 3(a) and figure 3(b) display our contacts for our Al/Si/Al and Ta/InAs junction, respectively. Ti/Au contact pads were deposited via *ex-situ* electron beam evaporation. With this setup, a current could be sourced through two electrodes whereas the other two electrodes could be used to sustain a voltage drop.

Ta/InAs junctions contained an additional Ti/Au contact as seen in figure 3(b) allowing for a gate voltage, V_g, to be applied over the semiconductor region for certain measurements. $V_g = 0$ for those measurement not requiring a gate voltage.

III. RESULTS AND DISCUSSION

A. Al/Si Josephson Junction

In our Al/Si/Al junctions, we utilized standard current bias measurements to generate I-V plots as shown in figure 4 in an effort to show both capacitive and tunneling properties. Specifically, we measured samples with varying junctions areas all corresponding to roughly the same fin thickness as seen in figure 3(a).

In figure 4(a) we show a standard I-V plot for our largest junction area of 22 μm^2 for both an up and down sweep of current. We note a hysteresis effect in our sample that is likely due to charge build up on the capacitor due to current sweeping. Thus, our capacitor is likely leaky, more closely resembling a capacitor with a parallel resistor. More importantly, there is no flat region of this graph; in other words, there is no current region corresponding to a resistance value of zero. While there is some current value corresponding to $V = 0$ in our down sweep, there is no extended current range with zero voltage, which would preferably be around $I = 0$. Thus, for our largest junction area, we do not see supercurrent in our sample. On the other hand, a flat region of zero resistance would be a strong indicator of tunneling.

In figure 4(b), we display the I-V plot for the various junction areas measured. In this figure, we only display the up sweep of current, but do note the presence of a hysteresis affect for all samples. It appears that at negative current values the voltage measured decreases with smaller junction area, but the pattern becomes somewhat irregular at positive current values. Again, for all junction areas, there are no regions of zero resistance. Thus, for all samples measured, we do not see any evidence of supercurrent.

Overall, we believe our Si fin barrier was simply to thick to support tunneling, and was at least 20 nm. As mentioned in section II A, part of the fabrication process entails repeated oxidation and etching of the Si fin to reduce thickness. With a estimate of the oxidized layer, and the number of etching cycles used, we can calculate a rough estimate of the thickness of the Si fin. It is quite difficult to obtain more accurate thickness measurements due to the scale of the fins. Tunneling electron microscopy (TEM) provides accurate measurements of the fin thickness, but destroys the sample in the process, whereas scanning electron microscopy (SEM) leaves the sample intact with quick feedback, but with less accuracy. With the samples measured here, it is likely more etching cycles were necessary to achieve fins supporting tunneling.

There are additional techniques that can be used to achieve the thinnest possible Si fins, but are not the most efficient. This involves staggered etching of Si fins until a fin breaks, ensuring its neighbor fin that has undergone one less etch is the thinnest possible. While this ensures the fin is as thin as possible, it involves the destruction of some samples.

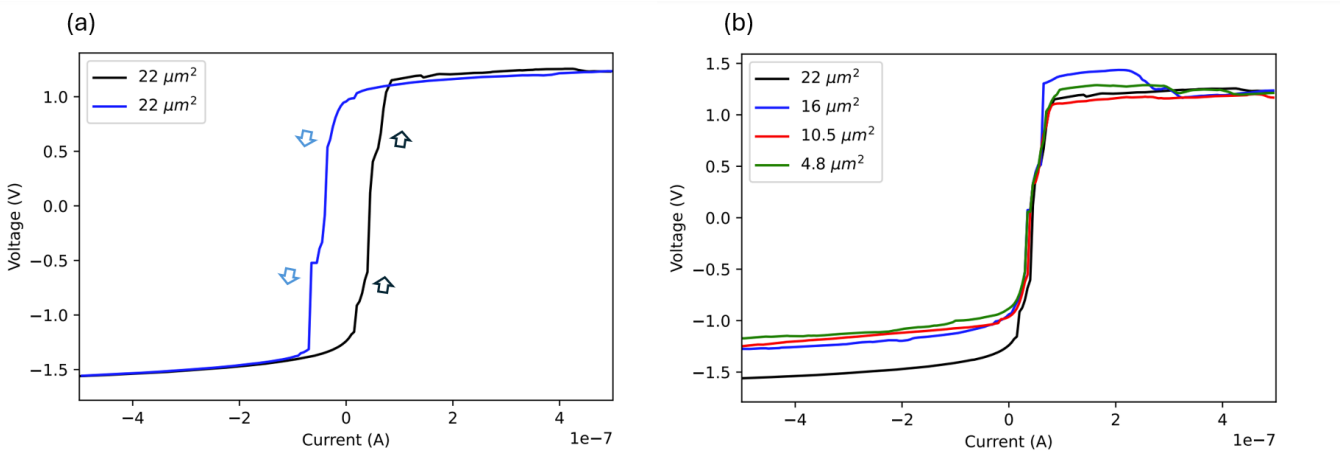

FIG. 4. Current bias measurements for Al/Si/Al junctions of different areas taken at $\sim$ 120 mK. (a) Voltage plotted as a function of current bias for thickest junction area of 22 μm^2 for both an up (black) and down (blue) current sweep. (b) Voltage plotted as a function of current bias for various junction areas, all in an up sweep of current.

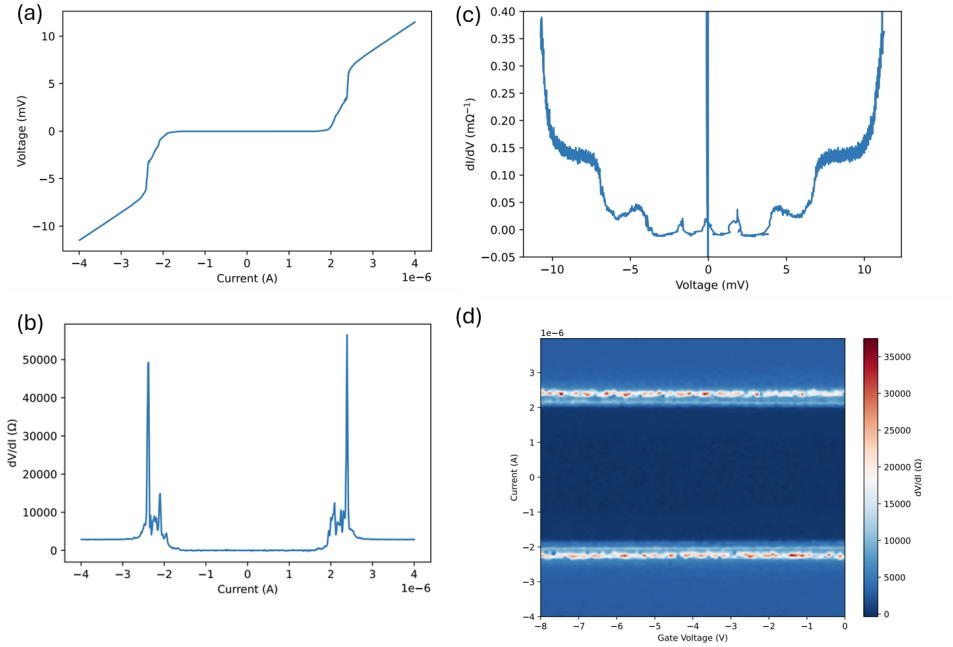

FIG. 5. I-V characterization with current and voltage bias, and current bias with gate voltage of Ta/InAs JJ. (a) Voltage characterization with current bias taken at $\sim$ 70 mK. (b) Differential resistance characterization with current bias taken at $\sim$ 70 mK. (c) Differential conductance characterization with voltage bias taken at $\sim$ 60 mK. (d) Differential resistance plotted against gate voltage and current bias in a 2D contour plot taken at 100-200 mK.

B. Ta/InAs Josephson Junction

All measurements pertaining to our Ta/InAs were done with the sample setup as shown in figure 3(b). We start with the standard figure of merit for a JJ, the product of I_c and the normal state resistance, R_N, which reveals the quality of the 2DEG layer by determining its transport regime.

Looking at figure 5(a), we plot voltage as a function of current bias and notice a region of zero resistance extending from -1.5 μA to 1.5 μA indicating the superconducting regime. From this we can extract I_c of $\sim$ 1.5 μA. As the current increases past I_c, we enter into a nonlinear regime and finally into a linear, resistive regime where extrapolation of the slope at these high current values yields $R_N \sim 2870\ \Omega$.

We find $I_c R_N = 4.4$ mV which can be related to the superconducting energy gap by the formula $I_c R_N = \alpha \Delta_0 / e$

where Δ_0 is the superconducting energy gap and α takes on the value of π and $1.32(\pi/2)$ for the ballistic and diffusive regime, respectively [21, 22]. The superconducting energy gap, Δ_0, can be calculated according to BCS theory by $2\Delta_0 = 3.5kT_c$ where T_c is the critical temperature of Ta of approximately 4.4 K [23]. We find $\Delta_0 = 0.6$ meV. Using these values presented, we find I_cR_N is 317% of the diffusive limit, indicating ballistic transport is probable and the 2DEG layer is of good quality.

Another useful product is $I_{ex}R_N$ where I_{ex} is the excess current flowing through the junction and is defined as $I_{ex} = I - V/R_N$ where I and V values are taken from the high current, resistive regime [17]. This product informs us of the quality of the S-Sm interface by determining the transport regime of the region. We find $I_{ex} = 8$ nA and $I_{ex}R_N = 26$ μV. The product $I_{ex}R_N$ is related to a similar formula, that being $I_{ex}R_N = \alpha'\Delta_0/e$ where α' takes on the value of 1.467 and 8/3 for a diffusive and ballistic junction, respectively [17, 24]. Surprisingly, we find $I_{ex}R_N$ is 2.5% of the diffusive limit indicating the diffusive regime is probable. This would seem to suggest our S-Sm interface is of bad (poor interface) quality, but further analysis suggest otherwise.

As mentioned, there is a nonlinear region in figure 5(a) that is better visualized in figure 5(b) with a plot of differential resistance versus current bias. There are a series of smaller peaks and valleys followed by a large peak. We attribute the large peak to the Ta transition, meaning at this high current value, Ta is exiting the superconducting regime. Normally, at currents exceeding I_c, superconducting Cooper pairs and single electrons tunnel through the junction [25], but we believe due the Ta transition peak, only single electrons are tunneling. Such would explain the extremely small value of I_{ex} calculated prior. We attribute the smaller peaks and dips in figure 5(b) to multiple Andreev reflections (MAR), a repetitive process at S-Sm interfaces where incident electrons at energies less then twice the superconducting gap form Cooper pairs in the superconductor with a resultant hole of opposite spin and momentum, and confirm our suspicion in figure 5(c).

Specifically, figure 5(c) plots differential conductance as a function of voltage bias. In this plot, we see a series of evenly spaced peaks a dips, a typical indication of the MAR process following $V = 2\Delta_0/en$ where n is an integer corresponding to the Andreev reflection peak [11]. These voltage peaks occur from 0-5 V, the same voltage range corresponding to the nonlinear regime in figure 5(a). Using the values of the voltage peaks, and their corresponding n value, we can calculate the expected value of the superconducting energy gap to compare with BCS theory. Doing so, yields an expected value of the gap of in the range of 1-4 meV where the value according to BCS theory was calculated prior and is about 0.6 meV. For detailed analysis on the MAR process in similar JJ-FETs, consult Ref. [11].

Crucially, the MAR process typically manifests itself in high quality (transparent) junctions. We believe the calculations involving the product of $I_{ex}R_N$ lead us to a false conclusion of poor interface quality, whereas observation of the Ta transition peak and observation of the MAR process start to reveal otherwise. This poses on an interesting avenue to explore the current range in figure 5(a) of 2-2.5 μA corresponding to the Andreev reflection regime, where Ta is superconducting. Thus, we define a new quantity, $I^*_{ex} = I^* - V^*/R_N$, modified from Blonder *et al.* [17], where I^* and V^* are chosen from the current range mentioned, allowing for the calculation of I^*_{ex} while Ta is superconducting. We speculate at this range Cooper pairs and single electrons are tunneling through the barrier, making the calculation of I^*_{ex} more meaningful than the calculation of I_{ex}. Specifically, we find $I^*_{ex} \sim 2$ μA, and the product $I^*_{ex}R_N = 5.7$ mV. Following the same methodology outlined prior, where now we have $I^*_{ex}R_N = \alpha'\Delta_0/e$, we find $I^*_{ex}R_N$ is 517% of the diffusive limit. This is another clue, indicating that ballistic transport is probable at the S-Sm interface.

While initial calculations involving $I_{ex}R_N$ may lead to a false conclusion of poor interface quality, further analysis has revealed otherwise. The Ta transition peak, not observed in similar Al junctions, sheds light on the small value of I_{ex}, while observation of the MAR process directed us to infer high interface quality. Using the product $I^*_{ex}R_N$, we confirm our belief of high interface transparency. Overall, this conclusion is noteworthy for similar devices utilizing superconducting Ta at a comparable current ranges.

Lastly, in figure 5(d), we plot differential resistance versus current and V_g in a 2D contour plot. The dark region in the center indicates zero resistance and hence the superconducting regime. As current increases, we can see an area of high resistance indicated by the red color, followed by a resistive regime indicated by a light blue color, a pattern closely matching that observed in figure 5(a) and figure 5(b). We find I_c to be the same as the value extrapolated from figure 5(a).

For a JJ-FET, we would expect at higher values of V_g the resultant electric field would deplete the semiconductor region, eventually shutting off the junction. This would manifest as a closure of the superconducting region, and continual smaller values of I_c as V_g is increased. Figure 5(d) displays a constant I_c with no closure of the superconducting regime. We postulate our InAs top layer contains an In rich surface reconstruction due to the samples overall preparation, which can effectively screen the resultant electric field stemming from the applied gate voltage. Reflection high energy electron diffraction (RHEED) is a technique that uses high energy electrons to study the morphology of growing thin films, and confirms our suspicions. Specifically, it yields a (4x2) surface reconstruction, consistent with the energetically favorable In rich reconstruction [26]. Alternative sample preparations should yield the desired (2x4) surface reconstruction, consistent with an As reconstruction.

IV. CONCLUSION

In this paper, we present our findings measuring Al/Si/Al and Ta/InAs Josephson junctions at low temperatures. For our Al/Si/Al junctions we find that for all junction areas, there is no evidence of tunneling (supercurrent) due to the fins thickness which can be addressed in the fabrication process. While we used standard techniques to indicate the quality of the 2DEG region in our Ta/InAs junction, determining S-Sm interface quality required more in depth analysis through which we ultimately conclude high interface quality. Furthermore, our findings indicate no tunability over the semiconductor region due to an In rich InGaAs top layer.

Broadly, utilizing crystalline barrier materials are an encouraging solution to tackling qubit loss and improving coherence times. Tunneling properties with a crystalline barrier has not been shown in a MET device. While our Al/Si/Al MET does not illustrate tunneling, we briefly mention alternative fabrication techniques promising in further reducing Si fin thickness, crucial for successful realization of such devices. Tunability is a key feature of JJ-FETs, and while there is not evidence of tunability in our Ta/InAs sample, alternative sample preparation methods are promising. Moreover, we present detailed analysis on Ta/InAs sample quality noticing phenomena not observed in similar Al/InAs junctions, namely a transition peak. Characterization methods outlined here are crucial for confirming sample quality, a necessary step for creating low loss superconducting qubits.

V. OUTLOOK

While there are steps in place to work further towards tunability in our Ta/InAs junction and tunnleing in our Al/Si/Al junction, here we present the impact of our work.

Our findings indicate a high quality Ta/InAs structure, grown with a shadow mask MBE technique. While shadow mask technology is not a novel technology, such high quality junctions have not been demonstrated with the technique. Crucially, we demonstrate shadow mask technology as a viable means to create high quality heterostructures. Shadow masking is an inherently *in situ* technique, can aid in the fabrication of devices not feasible with *ex situ* techniques [27], and has even been employed in various areas such as quantum dot construction [28]. For the purposes of JJ-FET fabrication, this poses an interesting avenue to explore growth of other promising superconducting materials such as Nb and TiN on our quantum well structure. Quality should not be impacted by the use of a shadow mask deposition technique.

Tunneling is likely to be shown with thinner Si fins, and will be a groundbreaking accomplishment in transmon qubit technology. This would create a compelling opportunity to explore other single crystalline barrier materials and other superconducting materials to further refine the device and aid in fabrication. Ge is an interesting candidate, gaining traction in CMOS applications for it superior qualities compared to established Si technologies [29]. It is particularly exciting for FinMET applications due its small band gap, meaning Ge fins conducive to tunneling could be thicker then their Si counterparts. Alternative sample materials like Ta could be explored for its superior native oxide properties [14, 15], aiding in further qubit loss reduction.

The work done here paves the way for additional material exploration to enhance the mentioned devices, with the ultimate aim of achieving practical quantum computation

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Appendix A: Differential Measurements

All measurements, including differential measurements utilized standard AC and DC lock in techniques.

To measure differential resistance, we sourced a DC current accompanied with a slight AC current of 10 nA, and measured the corresponding DC and AC voltage. The 10 nA AC current is our differential current ($\mathrm{d}I$), wheras the measured AC voltage is our differential voltage ($\mathrm{d}V$). Thus, with $\mathrm{d}I$, and $\mathrm{d}V$, we obtain differential resistance by $\mathrm{d}V/\mathrm{d}I$.

To measure differential conductance, we employed a similar method. Using a voltage divider to sustain voltage drops as low as 0.1 mV, we sustained by a DC voltage accompanied by a small AC voltage ($\mathrm{d}V$). We then measured the corresponding DC and AC ($\mathrm{d}I$) current, allowing us to obtain differential conductance, $\mathrm{d}I/\mathrm{d}V$. In theory, one should obtain differential conductance by inverting differential resistance, but to avoid unwanted noise we leveraged voltage bias measurements.

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